Translation

The following document is an example of a PRC provincial government plan to boost the semiconductor manufacturing industry. The highly granular and technical plan aims to elevate the quality of Guangdong Province's general purpose and specialized microchips to the leading level in China, and in some cases, to the global cutting edge.

Title
Application Guidelines for the "Chips, Software, and Compute" (Chip Category) Major Special Project of the 2020 Annual Guangdong Provincial Program for Research and Development in Key Fields
2020 年度广东省重点领域研发计划 “芯片、软件与计算”（芯片类）重大专项 申报指南

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The Chinese source text is available online at:
http://gdstc.gd.gov.cn/attachment/0/398/398724/3061058.pdf
An archived version of the Chinese source text is available at: https://perma.cc/CAD4-QY3H
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Translation Date	**Translator**	**Editor**
June 15, 2021	Etcetera Language Group, Inc.	Ben Murphy, CSET Translation Lead

Attachment 1[1]

Application Guidelines for the "Chips, Software, and Compute" (Chip Category) Major Special Project of the 2020 Annual Guangdong Provincial Program for Research and Development in Key Fields

[1] Translator's note: The following translation is an attachment to a notice (http://gdstc.gd.gov.cn/pro/tzgg/content/post_3056090.html; archived at https://perma.cc/CZA4-GN33) posted on the website of the Guangdong Provincial Science and Technology Department announcing the "Chips, Software, and Compute" Major Special Project of the 2020 Annual Guangdong Provincial Program for Research and Development in Key Fields.

The 2020 “Chips, Software, and Compute” (Chip Category) Major Special Project aims at international cutting-edge [research]. These projects are guided by national strategy and the major development needs of Guangdong and have the goal of improving the independent controllability (自主可控能力) of the core technology of the integrated circuit (IC) industry. They focus on the key links and the industrial ecosystem of IC design, manufacturing, and packaging and testing, gather superior Chinese teams to organize core technology research, strive to break through a number of major technical bottlenecks that restrict the innovation and development of the IC industry, place independent (自主) intellectual property rights in our hands, and achieve a number of landmark results.

In 2020, a total of 17 project directions will be established under the five themes of electronic design automation (EDA) technology R&D and application, IC manufacturing processes, heterogeneous packaging technology, equipment and parts, and the industrial innovation ecosystem. It is planned to support no more than 22 projects, with project implementation cycles of 3 to 4 years. Theme 1 Project 4 and Theme 2 Project 2 select organizations (单位) with advantages in this field to commission them for project implementation.

Theme 1: EDA technology R&D and application (theme no.: 20200127)

Project 1: EDA technology innovation and application in digital chip design

(i) Research content

With the aim of improving the design level of Guangdong’s digital microchips (including but not limited to: central processing units [CPUs], graphics processing units [GPUs], field-programmable gate arrays [FPGAs], and other high-end general purpose chips, various types of processors, Internet of Things [IoT] intelligent hardware core chips, automotive-grade artificial intelligence [AI] chips, and other special chips, as well as system-level system on a chip [SoC] chips for communication, AI, ultra-high-definition [UHD] video, automotive, satellite applications, smart home, intelligent healthcare, electronic office, and other fields) and through the optimization and innovation of EDA tools, projects will focus on supporting breakthroughs in core and key chip technologies such as custom architecture, chip security, low power consumption, heterogeneous computing, and hardware acceleration. Projects will carry out research on IC design methodologies, carry out technological innovation for design methodology problems such as changeable design processes, high timing closure requirements, high wiring density, and highly complex function and performance verification in the design of advanced node digital chips, and develop EDA tools related to the core and key technologies of chip design, including but not limited to design

process automation, hardware description and high-level integrated programming language and formal verification, programming model and compilation mapping (编译映射), logic simulation, logic synthesis, simulation verification, placement and routing, and other tools.

Projects will promote and apply developed innovative EDA tools to the design of digital IC chips, improve the design quality and efficiency of 100 million-logic-gate-level (门级) digital chips, and verify and optimize EDA tools during the chip design process.

(ii) Assessment indicators

Upon project completion, it must cover indicators 1, 2, and 4, and the indicators corresponding to the selected target chip product in indicator 3.

1. With at least one 100 million-logic-gate-level high-end chip application with international competitiveness as the background, projects will form EDA innovation technology and related tool development for this high-end chip and apply it in this chip.
2. The developed EDA tools will target process nodes of 14 nanometers or better. The performance and key technical parameters of more than one-point tools (一个以上点的工具), such as high-level synthesis, functional simulation, and timing simulation, will be benchmarked against existing or similar foreign tools to achieve leadership in China and an advanced level internationally, with some striving for international leadership.
3. By benchmarking against existing Chinese and foreign CPUs, GPUs, FPGAs, and other high-end general purpose chips, various types of processors, IoT intelligent hardware core chips, automotive-grade AI chips, and other chips, as well as system-level SoC chips for communication, AI, UHD video, automotive, satellite applications, smart home, intelligent healthcare, electronic office, and other fields or similar chips, the parameters and performance of key chip technologies such as custom architecture, information security, low power consumption, heterogeneous computing, and hardware acceleration will attain domestic leadership and an internationally advanced level. Information security chips must support the state secret algorithm system (国密算法体系); automotive-grade AI chips must meet Automotive Electronics Council AEC-Q100 grade 3 standards, and the target detection time must be less than 100 ms; and for IoT chips, the main frequency must exceed 200 MHz and they must support digital signal processing and floating-point operations.
4. Projects should apply for at least 10 national invention patents, at least 2 software copyrights, and at least 5 Patent Cooperation Treaty (PCT) patents.

(iii) Application requirements

Companies must take the lead, with chip design organizations encouraged to

cooperate with EDA tool research and development (R&D) units. EDA tool R&D units should undertake no less than 20% of the workload.

(iv) Level of support

The plan is to support 2 to 3 projects, with a funding amount not exceeding Chinese yuan Renminbi (RMB) 10 million per project.

Project 2: EDA technology innovation and application in analog or digital-analog hybrid IC chip design

(i) Research content

With the aim of improving the design level of Guangdong's analog and digital-analog hybrid chips (including but not limited to: chips for power devices, sensors, radio frequency [RF] circuits, display drive circuits, power management circuits, and millimeter wave circuits) and through the optimization and innovation of EDA tools, projects will focus on supporting breakthroughs in core and key chip technologies such as new processes, new architectures, signal integrity, chip stability, and heterogeneous integration. Projects will carry out research on IC design methodologies, carry out technological innovation for design methodology problems such as the low degree of automation in the design of analog and digital-analog hybrid IC chips at advanced process nodes or special process nodes (特色工艺节点) and the high complexity of computer simulation and verification, develop EDA tools related to the core and key technologies of chip design, including but not limited to tools for design process automation and circuit simulation analysis, focus on breaking through the traditional setting, perspective, intervention, comparison, and evaluation (SPICE) framework, and achieve simulations accurate to within 10% of the measured circuit performance.

Projects will promote and apply developed innovative EDA tools to the design of analog and digital-analog hybrid IC chips, improve the cost-efficiency of such chips, and verify, optimize, and apply EDA tools during the chip design process.

(ii) Assessment indicators

Upon project completion, it must cover indicators 1, 2, and 4, and the indicators corresponding to the selected target chip product in indicator 3.

1. With at least one mainstream high-end chip application with international competitiveness as the background, projects will form EDA innovation technology and related tools for this high-end chip and apply it in this chip.
2. The developed EDA tools will target process nodes of 16 nanometers or better. The performance and key technical parameters of more than one-point tools, such as circuit simulation, layout design, and parameter extraction, will be benchmarked

against existing or similar foreign tools to achieve leadership in China and an advanced level internationally, with some striving for international leadership.

3. By benchmarking against existing Chinese and foreign power semiconductor, RF, sensor, amplifier, display driver, power management, and millimeter wave chips or similar chips, the parameters and performance of key chip technologies such as new processes, new architectures, signal integrity, chip stability, and heterogeneous integration will attain domestic leadership and an internationally advanced level. For baseband chips and RF chips, mainstream Sub-6G low-frequency bands and the 28 GHz high-frequency millimeter wave band must be supported.
4. Projects should apply for at least 10 national invention patents, at least 2 software copyrights, and at least 5 PCT patents.

(iii) Application requirements

Companies must take the lead, with chip design organizations encouraged to cooperate with EDA tool R&D units. EDA tool R&D units should undertake no less than 20% of the workload.

(iv) Level of support

The plan is to support 1 to 2 projects, with a funding amount not exceeding RMB 10 million per project.

Project 3: EDA technology innovation and application in memory chip design

(i) Research content

With the aim of improving the design level of Guangdong's memory chips and through the optimization and innovation of EDA tools, projects will focus on supporting breakthroughs in core and key chip technologies such as new protocols, integration of memory and computation, physical unclonability, large capacity, self-correction, and stability. Projects will carry out research on IC design methodologies, carry out technological innovation for design methodology problems such as transistor density, low design margins, and process deviations with a major impact on chip quality and yield in advanced node (14nm or below) memory chip design, develop EDA tools related to the core and key chip design technologies, including but not limited to memory compilers, high-precision simulation tools, and rapid verification tools, and make full use of the highly structured characteristics of memory chip arrays. Through innovative technologies such as network division, model reduction, and ultra-large-scale parallelization, projects will improve simulation efficiency, capacity, and speed while maintaining sufficiently low precision requirements. Projects will research new technologies such as the fast Monte Carlo method to improve the

accuracy and speed of high-sigma verification.

Projects will promote and apply developed innovative EDA tools to the design of advanced memory chips such as flash memory, dynamic random access memory (DRAM), static random access memory (SRAM), and magnetoresistive random access memory (MRAM), improve the design quality and efficiency of such chips, and optimize and apply EDA tools during the chip design process.

(ii) Assessment indicators

Upon project completion, it must cover indicators 1, 2, and 4, and the indicators corresponding to the selected target chip product in indicator 3.

1. With at least one high-end memory chip application with international competitiveness as the background, projects will form EDA innovation technology and related tools for this chip and apply it in this chip.
2. The developed EDA tools will target process nodes of 14 nanometers or better. The performance and key technical parameters of more than one-point tools, such as memory compiler and simulation verification tools, will be benchmarked against existing or similar Chinese or foreign tools to achieve leadership in China and an advanced level internationally, with some striving for international leadership.
3. By benchmarking against existing Chinese and foreign chips or similar chips, the parameters and performance of key chip technologies such as new protocols, integration of memory and computation, physical unclonability, large capacity, self-correction, and stability will attain domestic leadership and an internationally advanced level. Solid-state storage (SSS) control chips must implement fully hardened elliptic-curve cryptography (ECC) and low-density parity-check (LDPC) algorithms and support the state secret algorithm system; flash memory chips must attain a leading triple-level cell/quad-level cell (TLC/QLC) layer number in China, with a continuous reading speed not less than 560 M/s and a continuous writing speed not less than 350 M/s.
4. Projects should apply for at least 10 national invention patents, at least 2 software copyrights, and at least 5 PCT patents.

(iii) Application requirements

Companies must take the lead, with chip design units encouraged to cooperate with EDA tool R&D units. EDA tool R&D units should undertake no less than 20% of the workload.

(iv) Level of support

The plan is to support 1 project, with a funding amount not exceeding RMB 10

million per project.

Theme 2: IC manufacturing processes (theme no.: 20200128)

Project 1: Research and development of precise device models and process design kit (PDK) process libraries based on simulated special processes

(i) Research content

With the aim of focusing on improving Guangdong's analog chips, especially the design of high-end digital-analog hybrid chips and their engineering design level, projects will make breakthroughs in featured analog semiconductor processes, precise device physical models based on the featured analog processes, and PDK process libraries for chip design. Proceeding from the nature of semiconductor materials, projects will carry out physical research on basic devices and make breakthroughs in reproducible key technologies from featured processes and physical device models to chip design. Centering on the design requirements of high-performance digital-analog hybrid chips and the industrialization "bottleneck," projects will focus on the R&D of physical device models that can accurately reflect featured processes (including different bias states, temperature conditions, processing angles, and process fluctuations) as well as related noise models and reliability models. Projects will build flexible, streamlined, and efficient compact models of semiconductor devices, especially models of active devices (有源器件), be able to achieve rapid integration with various EDA tools, improve simulation efficiency, and optimize the convergence speed of models. Projects will further establish PDK process libraries for chip design based on special processes and models of at least one typical chip and develop high-end digital-analog hybrid chip products including but not limited to high-precision, low-drift voltage references, ultra-low offset voltage amplifiers, high-precision analog-to-digital and digital-to-analog conversion chips, and input/output (I/O) and electrostatic discharge (ESD) macro models in order to provide a platform for the precise overall simulation of chip design.

(ii) Assessment indicators

1. Projects will develop simulated special processes based on the mass production of a 12-inch production line. Further, based on this process, projects will develop precise and compact device models based on physical characteristics and parameter extraction methods for these models. They will establish accurate physical device models (including different bias states, temperature conditions, process angles, process fluctuations, noise models, and reliability models) that can be used to simulate chip design. For metal-oxide-semiconductor (MOS) field effect devices, products will research and develop key parameters of physical models and ensure the model and

device characteristics can be accurately fitted in the subthreshold region, linear region, and saturation region. They will ensure the accuracy of the design and simulation of high-precision ICs, with their technical level reaching a leading level in China.

2. High-performance voltage reference benchmark chip intellectual property (IP) core. Products will research and develop voltage reference chips that can be used in the -40 to 125°C range, with a temperature drift of less than 8 ppm/°C and a peak-to-peak value (VP-P) noise of less than 6V and ripple suppression greater than 80 dB at less than 10 Hz. Projects will integrate with digital chips to achieve the mass production and application of digital-analog hybrid chips with voltage references.
3. Projects will apply for at least 10 national invention patents and obtain demonstration applications in analog-to-digital converters (ADCs) and other chips.

(iii) Application requirements

Chip manufacturers must take the lead in project implementation.

(iv) Level of support

The plan is to support 1 project, with a funding amount not exceeding RMB 20 million per project.

Theme 3: Key technology for IC packaging (theme no.: 20200129)

Project 1: R&D and application of key heterogeneous integration technologies

(i) Research content

With a focus on the R&D of multi-device packaging of advanced fine circuit chip heterogeneous interconnection in the semiconductor industry, projects will carry out integration and innovation R&D based on advanced packaging technologies, such as three-dimensional packaging, fan-out packaging, wafer-level packaging, flip-chip packaging, dual-flat no-leads/quad-flat no-leads (DFN/QFN) leadless packaging, system-in-package (SiP), vacuum packaging, and micro-electro-mechanical system (MEMS) technology, and achieve innovations in functional component architecture, high-efficiency processor and memory interconnection between high-bandwidth chips with line widths and line spacings of 5 micrometers (μm) to 40 μm, and compact system integration. Projects will develop product applications in the fields of RF modules, power devices, sensors, memory units, and optoelectronic (光电) heterogeneous devices as well as integrated silicon devices and passive devices (such as large-capacity capacitors, special inductors, and filters). The technical indicators of the products will be better than those manufactured by traditional processes, and their technical level will reach a leading position in China. Projects will master core

manufacturing technologies, reserve intellectual property rights, and indicate the direction for mass production.

(ii) Assessment indicators

The line width and line spacing of heterogeneous interconnection lines should be between 5 μm and 40 μm, and the silicon wafer spacing should be less than 200 μm; the number of packaging and wiring layers should be 4 or more; processes should achieve panel-level fan-out packaging of 200 mm or more or heterogeneous integration of 3D packaging; under -40°C to 85°C temperature cycle conditions, the number of cycles should be more than 1,000; the anti-electromigration ability of heterogeneous interconnection should be greater than 500h given the conditions 85°C and 104 A/cm2; the bandwidth of signal processing (processor and memory device) should be greater than 15 GBps; RF modules (including power amplifier [PA], RF switches, and low-noise amplifiers), narrow-band IoT ICs, sensors, silicon optical devices, and passive devices should achieve heterogeneous integration and industrialization; in cost analysis reports, the cost advantage should be at least 30% superior to that of traditional packaging; projects should apply for at least 10 national invention patents and at least 5 PCT patents.

(iii) Level of support

The plan is to support 2 projects, with a funding amount not exceeding RMB 10 million per project.

Project 2: Panel-level process R&D for advanced fine circuit packaging

(i) Research content

Projects will develop and mass produce high-end packaging substrates such as rigid substrates, flexible substrates, and rigid-flex substrates based on high-density and fine-circuit panel sizes above 200 mm and promote the replacement of imports with independently controllable domestic versions (自主可控国产化) of high-density, high-precision (minimum line width and line spacing, soldering materials, perforations, etc.), and high-performance (low loss, high reliability, small size, and high frequency) packaging substrate manufacturing. Projects will develop the mass production of panel-level fan-out packaging RF and power devices and achieve the industrialization of a new panel-level fan-out packaging with high integration, small sizes, and competitive prices, with technological levels achieving leadership in China.

(ii) Assessment indicators

Upon project completion, select one of the following 1-3 product directions and complete the corresponding assessment indicators. Indicator 4 must be covered.

1. Rigid substrates: 2 to 14-layer substrates, the minimum thickness of which should be 200 μm or less; the minimum line width/line spacing should be 8 μm/8 μm or less; the soldering hole should be 50 μm or less, the solder thickness is 10 μm, and the precision should be within 3 μm. Rigid-flex substrates: substrates with 4-14 or more layers; the minimum line width/line spacing should be 8 μm/8 μm or less; the bend life (弯折寿命) should be no less than 10,000 times (bend radius R=0.5 mm).
2. Flexible substrates: transmission loss should be less than 0.03 db/mm (at frequencies of 0.2 to 18 GHz) or 0.05db/mm (at frequencies of 18 to 40 GHz).
3. Panel fan-out RF process: 2 or more layers, production methods other than direct compression molding, such as plastic packaging processes, should be implemented.
4. Projects should apply for at least 10 national invention patents and at least 10 PCT patents. The output value of projects should exceed RMB 1 billion during the implementation period.

(iii) Application requirements

Enterprises shall take the lead. Applications featuring joint industry-academia-research institute methods are encouraged.

(iv) Level of support

The plan is to support 1 project, with a funding amount not exceeding RMB 10 million per project.

Theme 4: IC equipment and parts (theme no.: 20200130)

Project 1: Remote plasma source R&D

(i) Research content

Projects will conduct research on high-frequency voltage-based direct current (DC) electrode negative voltage generation technology, positive ion bombardment electrode acceleration technology, dual high-frequency voltage ion bombardment and high-ion flux discharge coordinated control technology, remote large-diameter plasma generation, and remote stability maintenance technology; conduct research on ion density measurement, temperature measurement, spatial distribution uniformity measurement, and free radical measurement inside plasma, rotational energy band analysis with the aid of emission spectroscopy, and remote in-situ plasma diagnosis technology, X-ray spectroscopy, plasma image acquisition, and other in-situ testing and analysis technologies; develop remote plasma source equipment; and carry out demonstration applications in the chip manufacturing industry. The technical level will reach the leading level in China.

(ii) Assessment indicators

Upon project completion, a set of remote plasma source equipment prototypes with high density, high activity, high uniformity, and low pollution must be developed that support in-situ measurement of the plasma source, with an ionization output power of 600 W and a power range that can be extended to an extended power range of 3 to 200 W. In a 200 mm to 300 mm vacuum reaction chamber, they should have a gas pressure range of 3 Torr to 10 Torr, a gas flow rate of 2.5 slm, and an ionization rate greater than 94%. Projects should apply for 5 invention patents, the developed remote plasma source equipment should achieve large-scale mass production and sales as well as application demonstration, and the product sales revenue should be at least RMB 30 million.

(iii) Level of support

The plan is to support 1 project, with a funding amount not exceeding RMB 10 million per project.

Project 2: R&D and industrialization of high-temperature and high-precision molecular beam epitaxy source furnaces (分子束原炉)

(i) Research content

Oriented to the development needs of quantum devices, infrared and millimeter wave devices, and 5G communication technology, projects will carry out thermodynamic analysis of the heating units of molecular beam epitaxy (MBE) source furnaces, make breakthroughs in convex and concave heat shield technology and wide contact compensation thermocouple temperature control technology, achieve high-precision temperature measurement, temperature control, and thermal insulation structure designs for multiple temperature zones, develop high-temperature and high-precision MBE source furnaces with independent intellectual property rights, and carry out demonstration applications on domestic FW-VI MBE equipment, with epitaxial growth of high-quality materials such as GaAs, AlGaAs, and InGaAs. The technical level will reach the leading level in China and meet the preparation requirements of new devices.

(ii) Assessment indicators

Upon project completion, a set of high-temperature and high-precision MBE (molecular beam) source furnace prototypes with independent intellectual property rights must be developed, with dual-temperature zone heating and a beam source furnace heating temperature of ≥1400°C; temperature control accuracy of ≤±0.1°C; integrated water cooling and shutter, automatic control system, and a source furnace

vacuum better than $6x10^{-10}$ Torr. In the verification of GaAs-based epitaxial material growth in molecular beam epitaxy systems, the GaAs epitaxial wafer size should be greater than 2 inches, the material growth rate should be 0.1 to 2 μm/h, the film thickness nonhomogeneity should be ≤3%, surface defects (1 μm thickness for GaAs) should be ≤50/cm^2; electrical properties (2 μm thickness for GaAs): background carrier concentration should be n≤3×10^{14}/cm^3, and mobility should be μ_{300K}≥6000 cm^2/V.s, μ_{77K}≥60000 cm^2/V.s. GaAs two-dimensional electronic gas material: n≈5×1011/cm^2, μ_{300K}≥6000 cm^2/V.s, μ_{77K}≥150000 cm^2/V.s. AlGaAs epitaxial material: composition nonhomogeneity (Al content 30%) ≤ ± 2%. The MBE equipment supported by projects should achieve sales of RMB 30 million.

(iii) Level of support

The plan is to support 1 project, with a funding amount not exceeding RMB 20 million per project.

Project 3: R&D on silicon carbide high-temperature oxidation furnace equipment

(i) Research content

Projects will research and develop high-temperature oxidation furnace equipment, carry out research on technology to reduce the interface state density between the gate dielectric SiO_2 and silicon carbide (SiC) of the metal–oxide–semiconductor field-effect transistors (MOSFETs) of unipolar devices, and improve channel carrier mobility. Projects will adjust the carrier lifetime of the n-type drift region and the p-type hole injection region in the insulated-gate bipolar transistor (IGBT) structure of hybrid bipolar devices. Projects will improve mobility and reduce the conduction loss of the device. The carrier lifetime will be controlled within a certain range, the high frequency performance of SiC devices will be greatly improved, and the switching frequency characteristics of the device will be maintained while the turn-off loss is reduced, thereby reducing the power consumption of the device. The technical level will reach the leading level in China.

(ii) Assessment indicators

Upon project completion, a set of multi-chip high-temperature oxidation furnace prototypes for silicon carbide devices must be developed to form multi-chip high-temperature oxidation furnace design, manufacturing, and support oxidation process technologies with independent intellectual property rights. The oxidation process of the SiC high-temperature oxidation should have a maximum temperature of 1500°C, and the equipment should be able to operate long-term at 1350°C. The heating rate should reach 8°C/min, and the equipment should have alarm and interlock

protection functions, with an mean time between failures (MTBF) of >500h. Projects should support batch oxidation processing of 2", 3", 4", and 6" wafers (20 wafers or more per furnace). Dry oxygen (O_2), nitrous oxide (N_2O), nitrogen oxide (NO), nitrogen dioxide (NO_2), or wet oxygen (O_2+H_2O) can be used for oxidation.

(iii) Level of support

The plan is to support 1 project, with a funding amount not exceeding RMB 10 million per project.

Project 4: R&D of cryopumps for semiconductor equipment

(i) Research content

Projects will carry out research on the ultra-low temperature gas capture mechanism and specialized helium compressor technology of small Gifford-McMahon (G-M) cryocoolers and carry out model and design simulation for the cryocooler unit and the vacuum pumping unit; develop intelligent control systems for cryopumps and network cryopump group control systems with independent intellectual property rights; carry our research on large pumping capacity and rapid pressure recovery technologies and develop mass production technologies for core components such as thin-walled cylinders, ultra-low temperature (10K) regenerators, and ultra-low temperature (10K) sealing elements; and establish an evaluation system for cryopumps used for semiconductors and formulate relevant technical standards for cryopumps used for semiconductors. Projects will research and develop cryopump systems used for semiconductors and dedicated cryopumps for high-end equipment and Chinese-made semiconductor devices and carry out research on industrialized mass production. The technical level will reach the leading level in China.

(ii) Assessment indicators

Upon project completion, a special cryopump system for semiconductor equipment with independent intellectual property rights must be developed. The product performance test standards should meet the international standard International Organization for Standardization (ISO) 21360-1, so the system can be used for import substitution in the preparation of 12-inch semiconductors. The ultimate vacuum of the equipment should reach 5.0e-9 Torr, the air and argon pumping speeds should not be less than 1500 L/s and 1150 L/s, the argon pumping capacity should be 750 Std.L (less than 30 seconds for pressure recovery to 5.0e-7 Torr), the full and rapid regeneration times should not exceed 170 and 60 minutes respectively, and a prototype of the cryogenic vacuum pump should be completed. Projects should establish an evaluation system for cryopumps used for semiconductor equipment, apply for at least 5 invention patents related to cryopumps used for semiconductor

equipment, and form 2 technical standards. The project results should be used for demonstration and application in chip manufacturing enterprises in the province.

(iii) Level of support

The plan is to support 1 project, with a funding amount not exceeding RMB 10 million per project.

Project 5: High-precision maskless laser direct writing (直写制板) technology and equipment

(i) Research content

Projects will research the key process technology for high-performance laser direct writing equipment that can be used to stably produce high-precision IC masks, research the key technologies of laser beam collimation, beam expansion and focusing, lens design, electronic platform transmission control (mainly the speed and precision of the workpiece table), visual recognition and feedback control, splicing and engraving precision control, system control software design, and other stages, research whole-machine (整机) manufacturing technology, develop domestic high-precision maskless laser direct writing equipment with independent intellectual property rights, and carry out demonstration applications in the manufacturing of high-precision optical masks and sensor chips. The technical level will reach the leading level in China.

(ii) Assessment indicators

Upon project completion, high-precision maskless laser direct writing equipment must be developed. The direct writing speed should support 1350 mm^2/min, the graphic writing format should support 250 mm × 250 mm, the laser light source should support 355 nm, and the exposure resolution should reach 0.75μm. Equipment should support resolution rate automatic conversion according to different writing speeds, with a minimum resolution accuracy not less than 14nm and support for multiple exposure modes. Equipment should support real-time auto-focus, substrate surface roughness tracking, grayscale photolithography (at least 2048 levels), multi-exposure and multi-layer alignment engraving, warped substrate pattern photolithography, and other functions. Equipment should support multiple data input formats (DXF, CIF, GDSII, and Gerber files). Projects should form 5 or more demonstration applications in IC masks, MEMS devices, photonic chips, sensor chips, flexible electronics, binary optics, fan-out packaging, and other fields and apply for 5 national invention patents.

(iii) Level of support

The plan is to support 1 project, with a funding amount not exceeding RMB 10 million per project.

Project 6: R&D and industrialization of 300 mm graphic alignment (图形套刻对准) measurement equipment

(i) Research content

Oriented to the detection and measurement needs of Chinese 20-14 nm node ICs, projects will develop graphic alignment measurement equipment, make breakthroughs in key technologies, and obtain core independent intellectual property rights. Projects will complete the R&D of key technologies and core components, including high numerical aperture and high angular resolution scattering imaging technology, multi-channel high signal-to-noise ratio spectral signal extraction technology, high-precision etching measurement signal analysis technology, highly robust adaptive optical focusing technology, high-speed and high-precision wafer motion displacement control technology, and high-speed image data processing technology.

(ii) Assessment indicators

Upon project completion, a 300 mm graphic alignment measurement equipment prototype with independent intellectual property rights must be developed, and the technical level will reach the leading level in China. The prototype should basically achieve indicators that can compete with international products. The projects should support the sales of 300 mm graphic alignment measurement equipment. The wafer size of the equipment should be 300 mm, the optical numerical aperture should be ≥0.9, the measurement precision of etching should be ≤0.5 nm, the single-point measurement time for etching should be ≤0.75 s, the yield should be ≥90 WPH, the normal operation time should be ≥90%, the mean time between failures should be ≥800 hrs, and the mean time to repair should be ≤6 hrs. Projects should complete joint development with Chinese suppliers of key device components and complete the testing and verification of the devices in the mass production lines of Chinese chip manufacturers.

(iii) Level of support

The plan is to support 1 project, with a funding amount not exceeding RMB 10 million per project.

Theme 5: IC innovation ecosystem (theme no.: 20200131)

Project 1: Technology R&D and application for the Chinese computing chip ecosystem

(i) Research content

Projects will research independently controllable (自主可控) computing platform technology based on Chinese computing chips, carry out system architecture innovations for high energy efficiency and low power consumption, optimize chip designs, improve chip computing capabilities, and form independent intellectual property rights. For scenarios such as data center big data computing, distributed storage, and advanced RISC machine (ARM) native applications, projects will optimize branch prediction algorithms, increase the quantity of computing units, improve the memory subsystem architecture, and improve the performance of domestic chips. Projects will research and optimize the system adaptability and degree of integration of architecture innovation methods to achieve the heterogeneous integration of chips of different functional types. Projects will research the application migration technology and performance analysis and optimization technology required for demonstration applications, effectively carry out industrialization demonstration applications of computing platforms in related fields for key industries and key businesses, and enhance the competitiveness and industrial scale of Chinese computing platforms.

(ii) Assessment indicators

Upon project completion, it must achieve the iteration of Chinese computing chips, with a total bandwidth of 1.5 Tb per second, and pass inspection and certification by an authoritative third-party institution. Projects should support multiple virtualization technologies such as CPU core virtualization, memory virtualization, interrupt virtualization, and I/O virtualization, support memory protection technologies such as scrambling, descrambling and error correction, build an adapted test environment for products and applications based on Chinese computing platforms, achieve demonstration applications in at least one field such as taxation, operators (运营商), finance, public security, automobiles, and power grids, realize at least 1,000 chip applications, and form at least 3 standards and specifications.

(iii) Application requirements

Enterprises shall take the lead. Applications featuring joint industry-academia-research institute methods are encouraged.

(iv) Level of support

The plan is to support 1 project, with a funding amount not exceeding about RMB 10 million per project.

Project 2: Technology R&D and application for the satellite-based enhancement of high-precision and ultra-low power BeiDou chip ecosystems

(i) Research content

In response to the application requirements of domestic satellite navigation systems in key areas such as aviation, transportation, smart IoT, shipping, and emergency rescue, projects will develop a new generation of chips and modules for baseband signal processing, RF signal processing, multi-source fusion integrated positioning, and positioning and short message integration, and optimize and improve the ecosystem chains of domestic satellite navigation systems. Targeting current situations such as the insufficient positioning accuracy and poor anti-interference (抗干扰) capabilities of current terminal products, projects will make breakthroughs in key technologies such as high-precision satellite signal tracking, source identification, and anti-spoofing (防欺骗) and develop high-precision, anti-interference baseband signal processing chips and RF signal processing chips. In view of the high power consumption and large size of modules, projects will make breakthroughs in multi-source integrated positioning signal access, low-noise RF reception, and anti-interference technologies, and develop low-power, low-cost, multi-source integrated positioning chips. In response to application requirements such as high global coverage requirements and large global short message service system capacity for offshore fishing, shipping, and other fields, projects will make breakthroughs in technologies such as intelligent pose sensing (智能位姿感知) and selective frequency transmission and develop integrated positioning and short message chips. Projects will select one of the above-mentioned directions in which to carry out research, and the developed chip should pass testing and certification by an authoritative third-party institution and obtain large-scale application and promotion in specific civilian products.

(ii) Assessment indicators

Upon project completion, select one of the following 1-3 product directions and complete the corresponding assessment indicators, as well as those of Indicator 4.

1. High-precision, anti-interference baseband signal processing chips and RF signal processing chips: The anti-interference bandwidth of the satellite signal should be at least 20 MHz, the single-source anti-interference capability should have at least a 100 dBc signal-to-interference ratio, three-source anti-interference capability should have at least an 85 dBc signal-to-interference ratio, and the precision should be less than 1 meter without interference.
2. Low-power, low-cost, multi-source integrated baseband anti-interference positioning chips: Chips should be able to process information from at least three types of sensors. When using a small antenna, the outdoor positioning accuracy should generally be better than 1 m; the average power consumption should be less than 15 mW (excluding RF); and the bare size (裸片) of the chip should be less than 2.5mm x 2.5mm.

3. Positioning and short message integrated chips should be compatible with all the civilian frequency points of the world's four major systems, with over 50 tracking satellites simultaneously. They should support satellite-based augmentation system (SBAS) high-precision satellite navigation and positioning, with a positioning accuracy better than 2.5 meters. The module attitude accuracy should be better than 1 mil/3 m, with support for global short message communication and group communication.
4. In total, projects should apply for 10 national invention patents and at least 2 IC layout designs and form at least 1 relevant industry standard. The chips developed should pass testing and certification by an authoritative third-party institution, and the output value of chip modules and terminal products should be at least RMB 100 million.

(iii) Application requirements

Enterprises shall take the lead. Applications featuring joint industry-academia-research institute methods are encouraged.

(iv) Level of support

The plan is to support 1 project, with a funding amount not exceeding RMB 10 million per project.

Project 3: R&D and industrialization of high-performance electronic components in large-scale equipment

(i) Research content

High-performance processors and high-power drive devices, such as microcontrollers, analog-to-digital and digital-to-analog conversion devices, power managers, RF modules/chips, and power drive devices, are widely used in automotive electronic systems, air conditioning systems, and high-end TVs (such as 4K and 8K). They have a decisive effect on the cost and performance of the whole machine. This theme intends to focus on the high-performance ICs used in such devices to carry out R&D and make breakthroughs in high-performance electronic components. Projects will complete practical application and industrialization to form key technologies and products with intellectual property rights. For industrial controllers, analog-to-digital converters, processors, and other devices, projects will carry out system optimization and integration, make breakthroughs in innovative architectures, and achieve breakthroughs in computing power enhancement and advanced process manufacturing, system integration and development, and high-performance encoding/decoding. For power management chips, projects will make breakthroughs in improving the level of chip application in precision reference (精密基准) technology, high response and high reliability control technology, and noise and ripple suppression

technology. For power drive devices, projects will achieve breakthroughs in reliability, breakdown voltage, and operating junction (工作结) temperature increase.

Through the implementation of this project, large enterprises with broad industrialization foundations and good investment strength and R&D capabilities are encouraged to leverage their own application advantages, conduct R&D aimed at the most core components, and realize the domestic production of core semiconductor chips and components and the application of complete systems (整机系统).

(ii) Assessment indicators

The following assessment indicators are not limited to the industry directions, specific product types, and technical performance indicators listed below. The following assessment indicators are only used as an important reference during application. The project encourages the R&D and industrialization of high-performance components in large-scale equipment and major systems. During application, one product direction under other industries can be selected. However, the industry and device models must be clearly indicated, the main performance indicators must attain advanced levels in China, and the actual application indicators must be completed during the construction period.

1. Specialized television chips.

DC-DC chips should achieve high performance, ultra-low power consumption, and high efficiency at light load. Chips should support an analog dimming function and high-precision software dimming backlight function; comply with international testing standards such as Electronic Industries Association/Joint Electron Device Engineering Council (EIA/JEDEC); have a motherboard driver display resolution of at least 4K@60Hz; have a motherboard standby power consumption of less than 0.5 W; have an audio performance of at least 8 ohm 8W@1KHz; and have a signal-to-noise ratio of >60 dB. During the project construction period, the annual shipment volume should exceed 15 million units.

2. Specialized air conditioning system chips.

The chips should have a breakdown voltage of VB ≥600 V and a maximum operating junction temperature of TJ ≥150°C. The microcontroller unit (MCU) control chip should be resistant to ESD ≥ 8 KV, and the chip memory should be embedded with self-checking 512 K Flash-level 64 K SRAM. During the project construction period, a 500,000-unit application should be realized, and the technical indicators should attain the level of mainstream international products.

3. Specialized automotive electronic system chips

The chips should support AI-based image processing algorithms, with graphics

rendering capabilities of at least 1700M pixels/s. In the real-time transmission of massive data volumes related to navigation and feedback, the chips must support downlink/uplink peak rates that exceed those of long term evolution (LTE) and other standards (300Mbps/150Mbps), and the chips need to comply with the AEC-Q100 standard. During the project construction period, more than 500,000 onboard system applications should be realized.

(iii) Application requirements

Enterprises shall take the lead. Applications featuring joint industry-academia-research institute methods are encouraged.

(iv) Level of support

The plan is to support 2 projects, with a funding amount not exceeding RMB 10 million per project.