Re-Shoring Advanced Semiconductor Packaging Innovation, Supply Chain Security, and U.S. Leadership in the Semiconductor Industry

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Targeted investment incentives to increase U.S.-based advanced packaging capacity are also important for increasing semiconductor supply chain resilience.

IN THE UNITED STATES, BOTH THE SEMICONductor industry and the government are engaged in ambitious plans to expand domestic semiconductor manufacturing capacity. Previous CSET research has covered in detail these efforts to "re-shore" this manufacturing [1]. The research found that the Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Act incentives, if carefully targeted and augmented by adequate regulatory and workforce support, could reverse the observable decline in U.S. semiconductor manufacturing capacity since 1990. This paper expands on that work and argues that targeted investment incentives to increase U.S.-based advanced packaging capacity are also important. Historically, packaging was viewed as a labor-intensive and low value-added "back-end" activity (as opposed to high value-added "front-end" semiconductor fabrication). As a result, firms offshored these activities to overseas locations, primarily in Asia.

Two factors are driving a change in how packaging is viewed:

First, firms increasingly recognize how important packaging is to processing power,particularly as Moore's Law slows. As a result, firms are investing large amounts of capital to develop equipment, materials, and systems that support the advanced packaging ecosystem. Packaging was historically seen as a necessity to *maintain* thefunctionality of semiconductors. Advanced packaging is increasingly viewed as an opportunity to *advance the leading edge* in semiconductor technologies.

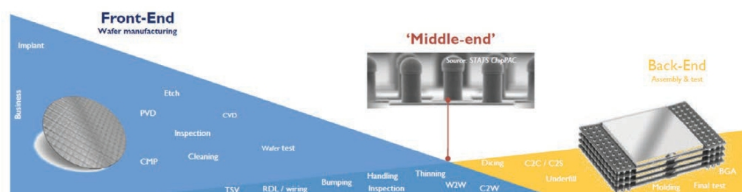


Figure 1. Advanced packaging, moving from back end to front end. Source: Kumar, Chitoraga, and Shoo, "Status of the Advanced Packaging Industry 2021," 214.

Packaging is becoming a bottleneck to semiconductor innovation because "densities of transistors in logic and memory chips have continued to increase exponentially, but the density of interconnects [wires] between logic and memory—governed by packaging— have increased at a much slower rate, leading to communication bottlenecks between chips." [2] The semiconductor industry has focused fewer resources on addressing this problem in favor of continuing traditional complementary metal-oxide semiconductor scaling as dictated by Moore's Law. However, as transistor density reaches physical limits, the industry seeks novel ways to increase chip performance. [3] New packaging techniques promise to increase interconnect density, which will accelerate signal speedand reduce energy requirements. [4]

Advanced packaging has entered the mainstream of the semiconductor industry. Leading firms are placing multi-billion-dollar bets on advanced packaging, and the technologies are

*This is a condensed version of the paper originally published on the CSET website. The full version can be found at https://cset.georgetown.edu/publication/re-shoring-advanced-semiconductor-packaging/

Table 1. Recent U.S. Legislation Related to Advanced Packaging

RELEVANT SECTIONS OF 2021 NDAA	COLLOQUIAL NAME	USICA FUNDING OF 2021 NDAA	USICA FY22 FUNDING	USICA FUNDING FY23–26
Section 9902	Mature Node Fabrication	Sec. 1002 (a)(3)(A)	$2 billion	N/A
Section 9903 (b)	DOD Microelectronics R&D Network	Sec. 1002 (b)	$400 million	$400 million per year
Section 9906 (c)(2)(A)(i)	National Semiconductor Technology Center	Sec. 1002(a)(2)(A)	$2 billion	Amounts divided between Section 9906 (c)/(d)/(e)/(f): FY23: $2B FY24: $1.3B
Section 9906 (d)	National Advanced Packaging Manufacturing Program		$2.5 billion	
Section 9906 (f)	Manufacturing USA Institute		$500 million	FY25: $1.1B FY26: $1.8B

Source: Author's compilation derived from Public Law No: 116-283 and S.1260 - United States Innovation and Competition Act of 2021.

poised to see adoption across a wide variety of electronic systems. Leading firms are attempting to cement their positions through strategic investments in advanced packaging today that will preclude competition tomorrow. Notably, these investments increasingly focus on automating the packaging process. Investments that develop packaging automation change the economic calculations that companies face when considering where to establish or expand packaging operations. As factories become more automated, labor costs become less of a factor in determining where to establish facilities. This trend is potentially favorable for U.S. re-shoring efforts, and the change has important implications, given ongoing unease among U.S. policymakers about the security of the semiconductor supply chain. Policymakers should craft incentives to re-shore advanced packaging capacity with these changing costs in mind.

Second, innovation in advanced packaging will be a key determinant of the depth and breadth of innovation in other emerging technologies. Currently, advanced packaging technologies are predominantly used in mobile and consumer electronic applications. Increasingly, however, these technologies will see widespread adoption in cloud computing, medical, automotive, and aerospace applications. [5] Advances in packaging amplify improvements in transistor density, and improvements in transistor performance have important implications for firm leadership in a wide variety of emerging technologies. Firms that lead in advanced packaging, along with systems that lead in incorporating advanced packaged technologies, will enjoy asymmetric performance advantages in the short and medium term.

U.S. Policy and Advanced Packaging

While the United States continues to lead in semiconductor design, it has seen a consistent decline in fabrication capacity. [7] U.S.-based ATP capacity has seen a similar decline. Though there are several dozen U.S.-headquartered packaging vendors capable of providing boutique low-volume services, North America's share of global packaging capacity is only 3 percent. [8] In general, U.S. firms (with the exception of Intel) lack high-volume packaging capacity, and the associated ecosystem (substrates,wafer bumping, equipment) is also lacking.

The CHIPS Act aims to reverse this trend. It includes several provisions related to advanced packaging. These represent a substantial effort by the U.S. government to establish and expand the advanced packaging ecosystem in the United States. Specifically, these provisions provide funding to establish a variety of advanced packaging research and development programs and could, theoretically, also be used to expand advanced packaging capacity in the United States, depending on how the funds are allocated and projects prioritized. Importantly, many of these provisions were funded as part of the U.S. Innovation and Competition Act (USICA), by the U.S. Senate in June 2021, which is now being reconciled in a conference committee with the America COMPETES Act passed by the U.S. House of Representatives in February 2022. [9]

USICA allocates $2 billion to provide federal assistance to incentivize

investment in facilities and equipment in support of the "fabrication, assembly, testing, or advanced packaging of semiconductors at mature technology nodes." [9] USICA also provides $400 million per year (FY22–26) to support the establishment and operation of a Department of Defense Microelectronics research and development network. Some of this funding could be directed toward advanced packaging research, given the myriad DOD electronics packaging requirements. Finally, USICA provides research and development investments in the form of $2 billion for a National Semiconductor Technology Center, $2.5 billion for a National Advanced Packaging Manufacturing Program, and $500 million for a Manufacturing USA Institute in FY22 to support advanced packaging, among other microelectronics research priorities. [10] Supplemental funding for these latter programs is also provided for FY23–26 to the tune of $1.1–$2 billion.

Re-Shoring Advanced Packaging in the United States

The aforementioned policies are all worthy aspirations, but the simple fact is that leading foundries and OSATs (nearly all of which are headquartered in Asia, as noted)have very little economic incentive to build an advanced packaging facility in the United States. The costs of re-shoring advanced packaging necessitate a well-definedstrategy that makes efficient use of funds to target specific technologies in the advanced packaging ecosystem. At the same time, the thinking behind this strategy should accept that the economics of re-shoring the broader ATP ecosystem prevent a return of meaningful capacity to the United States. Policymakers should accept that there is almost no economic case for re-shoring mature packaging technologies and instead focus on a strategy that targets advanced packaging specifically. The policy should consist of three pillars:

- Increase advanced packaging facility capacity in the United States
- Increase production of advanced packaging equipment and materials in theUnited States
- Target research and development that supports innovation in advanced packaging.

Increase advanced packaging facility capacity in the United States
Industry analysts expect that there will be 29 new fab construction projects started by the end of 2022. These 29 fabs are estimated to produce up to 14.5 million wafers per year (in 300 mm equivalents). [11] This increased wafer fabrication capacity necessitates more advanced packaging capacity in particular, and ATP capacity more generally, to maintain processing volumes. Current ATP capital expenditure investment levels will need to be sustained or expanded so that OSATs, IDMs, and foundries have the capacity in place to assemble, test, and package the increased wafer fabrication capacity as it comes on line. OSATs, IDMs, and foundries are all contemplating new construction of ATP facilities to meet this greater demand, and the United States should provide incentives to encourage firms to establish or expand ATP capacity domestically.

Congress is considering allocating billions of dollars directly and indirectly to support the advanced packaging ecosystem. In addition to the $2.5 billion National Advanced Packaging Manufacturing Program, which is primarily an R&D effort, several lines of funding identified by the CHIPS Act are available as incentives for advanced packaging facility construction. For example, if the $2 billion earmarked for "fabrication, assembly, testing, or advanced packaging of semiconductors at mature technology nodes" were to be directed specifically to advanced packaging support for mature nodes, these incentives would meaningfully encourage the establishment of new advanced packaging facilities in the United States. Except for Intel, no firms operate high-volume advanced packaging facilities in the United States. As a result, modeling the cost of a U.S.-based AP facility's construction and operations is difficult. Intel has previously estimated that it would cost $650–$875 million to relocate its ATP facility from China to another country. [12] Its public financial filings also indicate that it estimates the current value of its China-based ATP facility at around $851 million. [13] Meanwhile, Amkor recently estimated that Phase 1 of its new facility in Vietnam required initial capital expenditures of $200–$250 million. [14] In addition to the cost of construction, packaging facility costs must take into account reoccurring operations such as labor and utility rates, which vary substantially between Asia and the United States. [15]

In order to make these funds go as far as possible, policymakers should also direct incentives to foundries and IDMs that have plans to expand semiconductor fabrication capabilities in the United States, and should preferentially direct incentive funds to projects that include a front-end fab co-located with a back-end ATP facility, ideally anadvanced packaging facility. Large foundries and IDMs already prefer to co-locate theiradvanced packaging operations with the fabrication operations, and providing incentives for them to do so in the United States would maximize this return on investment. [16] Additional funds could be provided to leading OSATs interested in establishing advanced packaging operations in the United States. Importantly, there is a wide variety of techniques and technologies today that constitute advanced packaging, and no approach has emerged as dominant. As a result, policymakers should target incentives at firms that are providing a variety of packaging services, from wafer-level to

flip chip-BGA. These incentives could also be conditioned based on a facility's capacity, using as reference points cleanroom square footage and wafer processing size.

Increase supply of advanced packaging materials in the United States to reduce supply chain vulnerabilities IC substrates are of particular importance to advanced packaging, and in this market, the presence of U.S. firms as well as U.S. production is extremely limited. IC substrates are used in a wide variety of electronics destined for aerospace, in particular with military applications. The sole U.S.-based supplier of IC substrates suitable for advanced packaging reports that 36 percent of its total net sales (which included IC substrates and PCBs, among other electronic components) comes from the aerospace and defense market. [17]

Within the supply chain for advanced packaging, there is an especially acute shortageof the IC substrate material. [18] Of particular concern are Ajinomoto Build Up film substrates. These are used in packaging processes for high-end CPU, GPU and 5G networking chips by major chipmakers, including Intel, AMD, and Nvidia. [19] Fires in October 2020 and February 2021 at Taiwanese producers of substrates exacerbated this supply crunch, leading to delays of up to 40 weeks for certain substrates. [20]

Suppliers are investing up to $5 billion to expand FC-BGA substrate capacity, but more capacity will be available by late 2022 at the earliest, and it is all located outside the United States. [21] An advanced substrate processing facility costs $300 million (Intel has estimated $1 billion), and the equipment to operate such a facility currently has a two-year lead time. [22] In spite of the anticipated capacity expansions described here, one industry association estimates that increased capacity will meet just 78 percent of demand for these substrates by 2025. [23]

One industry association also found that the barriers to entry for the FC-BGA substrate market include an investment of more than $1 billion, market leaders' 20-year head start, and the need for a 1,000-person workforce for every facility. [24] Conversely, a South Korean PCB manufacturer recently opened a new facility in Malaysia at a cost of $121 million and reported that it will produce both PCBs and substrates. [25] Given the increasing importance of substrates, some funds could be directed to encourage the formation of one or more joint ventures (either between an OSAT and a substrate supplier, a foundry/IDM and substrate supplier, or a substrate and PCB supplier) to increase domestic production of IC substrates.

Target research and development that supports advanced packaging Innovation in advanced packaging materials, equipment, and services is essential to future U.S. semiconductor leadership. Improvements that increase semiconductor performance while reducing power consumption, cost, and form factor should be prioritized. In addition, innovations that are easily commercialized, flexible, and scalable should be prioritized. [26] This section argues that the United States should fund advanced packaging innovations related to chiplets and heterogeneous integration, equipment automation, and wafer-level packaging based on these factors.

Chiplets and Heterogeneous Integration [27]

Chiplets have risen in popularity as the costs of producing leading-edge chips has increased, the number of firms capable of producing such chips has decreased, and Moore's Law has slowed. According to one firm, the semiconductor industry is in the process of "adopting a chiplet based approach to reduce the overall cost, improve the individual yields and deliver required performance." [28] Industry analysts expect that chiplets will be a key enabler of advances in semiconductors "for the next 10–20 years." [29] An industry consortium consisting of representatives from leading technology firms was recently established to standardize the chiplet ecosystem. [30]

A chiplet "is an integrated circuit block that has been specifically designed to communicate with other chiplets, to form larger more complex ICs. Thus, in large and complex chip designs the design is subdivided into functional circuit blocks, often reusable IP blocks, called 'chiplets,' that are manufactured and recombined on high density interconnect." [31] In essence, chiplets are a way to make an electronic system behave like it is one integrated circuit, when in fact it is composed of several different smaller integrated circuits. This is accomplished via heterogeneous integration, "the integration of separately manufactured components into a higher-level assembly (System in Package—SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics." [32]

Chiplets offer four main advantages: (1) they are small, which increases the number ofoperable chips per wafer ("yield") and thus economies of scale; (2) they allow for heterogeneous integration of advanced and mature-node chips on the same system, collectively increasing system performance; (3) customers can mix and match or customize various chiplets to optimize system performance for their specific applications; (4) chiplets enable a combination of disparate material systems (e.g., gallium nitride, or GaN) to provide better performance than using just silicon.

Advanced packaging systems, materials, and equipment are all essential for enabling the die-to-die interconnects on which chiplets rely. [33] While chiplets are not a package type, they make use of advanced packaging to integrate

different types of chips to form larger and more complex chips that have increased performance and functionality. [34] Increasing the adoption and consumption of chiplets will be contingent on advanced packaging innovations. AMD reports that its chiplet-based prototypes are 15 percent faster than its conventionally packaged equivalent offerings. [35]

Emergence of Fan-Out Wafer-Level Packaging

Fan-out wafer-level packaging (FOWLP) refers to the process of packaging a finished semiconductor die while still in wafer form, either singly or combined with additional dies or other components such as discrete passive devices, or functional components such as microelectromechanical systems or radio-frequency filters. [36] This allows the production of wafer- and panel-level packaging using heterogeneous integration. The main advantages of FOWLP are the "substrate-less package, lower thermal resistance,higher performance due to shorter interconnects together with direct IC connection by thin film metalization instead of wire bonds or flip chip bumps and lower parasitic effects." [37] Interestingly, unlike other parts of the semiconductor supply chain, the supply chain for FOWLP is expanding. Analysts assess that there were ~5 firms engaged in FOWLP in 2019, and this number has now grown to 11 in 2021. [38] The technology is being adopted and popularized by TSMC in particular, and is seeing increased adoption among its clients' systems as a result. [39] As of 2020, TSMC maintained 66.9 percent of the market share for fan-out advanced packaging. [40] Incentives should be directed to encourage TSMC to co-locate an advanced packaging facility with its Arizona fab to increase U.S. domestic capacity for wafer-level packaging.

One example of FOWLP's benefits that is particularly relevant to AI comes from the U.S. chip startup Cerebras. Cerebras designs so-called Wafer Scale Engines (WSEs),an application-specific integrated circuit that encompasses an entire wafer and is optimized for machine learning tasks. [41] However, as previously discussed, even the fastest chips are constrained by the input/output capacity of their packaging. As a result, reports indicate that Cerebras is partnering with TSMC (its fabrication partner)to develop a wafer-scale package using TSMC's fan-out process to preserve the size advantage/compute advantage that wafer-level processing creates, and to increase compute-related advances in artificial intelligence research and development. [42] One

U.S. Department of Energy laboratory reports that Cerebras's technology is providing modeling results 300 times faster than its previous system. [43] Further advances in howthese WSEs are packaged would increase speeds, and doing so in the United States would benefit innovative U.S. firms and government customers.

Advanced Packaging equipment innovation

As packaging techniques such as FOWLP increase in popularity, the equipment and tools that support them must necessarily innovate to meet the demand. Importantly, these innovations in equipment also mean that packaging will become increasingly automated, which potentially will change labor rates and their role in modeling future advanced packaging facility costs. In particular, wafer-level packaging places unique demands on equipment, because it necessitates verification that the fabricated wafercontains the maximum number of operable chips. This quality control step was traditionally considered a front-end semiconductor fabrication activity, but it is increasingly performed in support of back-end advanced packaging requirements.

These requirements have opened new business lines for large (primarily U.S.-based) suppliers of semiconductor manufacturing equipment. More and more, they are now offering products to serve the advanced packaging market (FIGURE 1). One example of this is California-based KLA, a supplier of quality and process-control equipment that leads the worldwide market for front-end meteorology equipment used in semiconductor fabrication. KLA has recently started providing high-sensitivity defect-detection tools for advanced wafer-level packaging. [44]

Back-end advanced packaging increasingly resembles front-end semiconductor fabrication in terms of its need for automation. The more advanced packaging can be automated, the more U.S. equipment firms will benefit and labor rates will decrease as a deciding factor when firms choose where to locate ATP facilities. The United States is poised to benefit from these trends and should make investments in support of it.

Recommendations

Based on observable industry trends and the analysis outlined in this paper, any effort to increase semiconductor supply chain resilience must take advanced packaging in to account. Below are several recommendations to inform this effort:

Leverage CHIPS Act funds to incentivize increased domestic advanced packaging capacity. Multiple provisions within the CHIPS Act *authorize,* but do not require, funds to be directed toward advanced packaging projects. To the extentpossible, policymakers should use this latitude to focus funds on effortsthat increase domestic advanced packaging capacity and research and development.

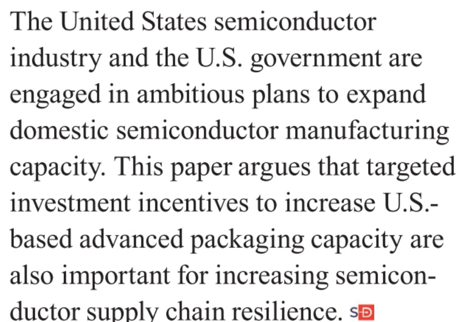
Preferentially direct CHIPS Act funds to semiconductor fabrication project proposals that include concurrent and co-located investments in advanced packaging capabilities. Large foundries

and IDMs such as TSMC, Samsung, and Intel already prefer to co-locate their advanced packaging operations with the fabrication operations, and providing incentives for them to do so in the United States would maximize this return on investment. For example, TSMC and Samsung have ongoing fab construction projects in Arizona and Texas respectively. Both companies have not announced plans to add an advanced packaging facility to their respective projects, but they should be encouraged to do so.

Encourage the formation of a U.S.-based joint venture with a leading supplierof IC substrates used in advanced packaging. The United States currently lacks sufficient variety and volume of IC substrate capacity to meet advanced packaging demand. Increasing domestic IC substrate capacity would improve advanced packaging supply chain resilience, and semiconductor supply chain resilience more generally.

Provide incentives that encourage at least one leading OSAT to establish an advanced packaging facility in the United States that provides commercially viable FC-BGA.

Use funds from the National Advanced Packaging Manufacturing Program to promote advanced packaging innovation. There is a wide variety of techniques and technologies today that constitute advanced packaging, and no approach has emerged as dominant. Policymakers should target R&D funds at firms and consortia that are providing a variety of packaging services, from wafer-level to flipchip-BGA. These incentives could also be conditioned based on facility capacity, using as reference points cleanroom square footage and wafer processing size. For example, funds could be used to: 1) Establish a public private partnership between U.S. OSATs and IDMs and a U.S. university that features a Class 10,000 cleanroom engaged in research and development of IC substrates and advanced packaging technologies. 2) Promote innovation in chiplets, wafer-level packaging, and packaging equipment automation.



Conclusion

The United States semiconductor industry and the U.S. government are engaged in ambitious plans to expand domestic semiconductor manufacturing capacity. This paper argues that targeted investment incentives to increase U.S.-based advanced packaging capacity are also important for increasing semiconductor supply chain resilience.

About the author

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Acknowledgments

For helpful feedback and suggestions, the author would like to thank Yan Zheng, Dan Wang, Igor Mikolic-Torreira, and Will Hunt. He would also like to thank Melissa Deng, Shelton Fitch, Lynne Weil, Dale Brauner, Danny Hague, and Adrienne Thompson for editorial support.

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