March 15, 2022

RFI Response: Supporting a Strong Domestic Semiconductor Industry—
Office of Policy and Strategic Planning, U.S. Department of Commerce
87 Fed. Reg. 3497; Docket No: 220119-0024

The Center for Security and Emerging Technology (CSET) offers the following submission for the consideration of the Department of Commerce. The Department of Commerce requested information "in order to inform the planning and design of potential programs to: Incentivize investment in semiconductor manufacturing facilities and associated ecosystems; provide for shared infrastructure to accelerate semiconductor research, development, and prototyping; and support research related to advanced packaging and advanced metrology to ensure a robust domestic semiconductor industry."

CSET has provided responses to questions where we believe CSET research is responsive or, in some cases, where we are aware of reliable research that has attempted to answer the question.

Summary of key points and recommendations

SEMICONDUCTOR FINANCIAL ASSISTANCE PROGRAM

- U.S. overdependence on the supply of leading-edge logic, DRAM, and legacy logic chipmaking capacity, as well as Assembly, Test, and Packaging (ATP) capacity in East Asia threatens U.S. economic and national security. The United States should therefore:
    - Focus CHIPS Act manufacturing incentives on leading-edge logic (first priority), DRAM (second priority), and legacy logic chips (third priority).
    - Increase advanced packaging facility capacity in the United States.
    - Increase supply of advanced packaging equipment and supplies in the United States.
    - Target research and development that supports innovation in advanced packaging.
- When reviewing applications for federal financial assistance, the Secretary should consider a range of factors that are not currently addressed in Section 9902 of the NDAA, including potential stipulations about covered entities, eligibility criteria, and relevant bidding categories.
- To maximize the initial scale of projects and to ensure ongoing reinvestment in project expansions, tool upgrades, and productivity improvements for the projects to remain economically viable and competitive over time, we suggest following the recommendations in a 2017 study by the Potomac Institute for Policy Studies[1]:

[1] https://potomacinstitute.org/images/studies/CARTSsm.pdf

    - Ensure that the funding level of any major public-private R&D initiative is at a magnitude that mirrors previous successful initiatives: $200-$300 million per year, 10-year timeline, total budget of $2-$3 billion.
    - Include costs for technology transition and insertion in all major public-private R&D program budgets.
    - Have government R&D efforts focus on low volume, customizable manufacturing solutions to technical challenges.
    - Use OTA acquisition mechanisms in all R&D programs.
- To ensure that semiconductor startups and small- and mid-sized companies have access to commercial fabrication, assembly, testing and packaging facilities and associated technical expertise, we suggest establishing the following facilities, as recommended in a 2021 study by In-Q-Tel[2]:
    - A national facility to field innovative semiconductor tools and fabricate next-generation microelectronics products in areas critical to national security
    - A fabrication sandbox to provide startups access to commercial equipment and tools, early design validation, and valuable testing data to share with potential investors while the government gains early access to innovative technology that could be tested against government requirements and inform future mission planning and acquisition needs
    - A dedicated Advanced Packaging facility that could test how U.S. chip designs work with Advanced Packaging processes and accelerate the transfer of technology from the lab, helping propel U.S. companies toward leadership in this emerging field.

ADVANCED PACKAGING MANUFACTURING PROGRAM

- The United States should focus funding for advanced packaging innovation on R&D related to chiplets and heterogeneous integration, equipment automation, and wafer-level packaging.
    - These areas of innovation promise to increase semiconductor performance while reducing power consumption, cost, and form factor should be prioritized.
    - They are also easily commercialized, flexible, and scalable.
- Given the increasing importance of IC substrates, some funding could be directed to encourage formation of one or more joint ventures (either between an OSAT and a substrate supplier, a foundry/IDM and substrate supplier, or a substrate and PCB supplier) to increase domestic production.

SEMICONDUCTOR WORKFORCE

[2] https://www.iqt.org/news/national-security-challenges-for-microelectronics/

- CHIPS Act manufacturing incentives will likely generate tens of thousands of new jobs, thousands of which will likely need to be filled by immigrants.
    - Experienced, high-skilled foreign talent will be especially needed for engineering roles, where we have estimated that employment could grow by 19 percent over the next decade.
- The United States can and should invest in growing the pipeline of American students in semiconductor-relevant graduate programs. Options for investment include:
    - K-12 STEM education
    - Funded 4+1 (undergraduate + master's) programs in semiconductor-related fields
    - On-the-job training programs to help graduates acquire the tacit engineering know-how required for many semiconductor manufacturing-related careers.
- The United States should also facilitate high-skilled immigration of foreign-born workers, especially those with experience in semiconductor engineering.
    - Policymakers should consider establishing an accelerated immigration pathway for experienced fab workers—perhaps specifically for Taiwanese or South Korean workers seeking to work in newly constructed fabs in the United States.
    - Caps on employment-based green cards should also be lifted for workers in the semiconductor industry, or perhaps for workers in national-security-relevant industries more broadly, if those workers have relevant master's or doctoral degrees. This will be particularly helpful for U.S. firms like Intel which currently employ many workers using employment-based green cards.

1. SEMICONDUCTOR FINANCIAL ASSISTANCE PROGRAM

1. The term "semiconductor" is not specifically defined in Section 9902 of the NDAA; rather, the legislation leaves it to the Secretary of Commerce to define. What factors do you consider important in developing a definition of "semiconductor" for purposes of a semiconductor manufacturing incentives program?

"Semiconductor" can be used to refer to a class of materials like silicon and germanium which can be either conductive and insulative under different conditions. But "semiconductor" can also refer to a class of electronic devices in which electronic conduction takes place within a semiconductor material. This latter usage is relevant for the purposes of a semiconductor manufacturing incentives program. For other definitional questions relating to the semiconductor industry, see https://ieeexplore.ieee.org/document/4114093.

3. Based on the criteria outlined in Section 9902 of the NDAA, what types of facilities, equipment, and other capacity aligned with the manufacture of semiconductors do you see as being most critical to the interests of the United States?

Overdependence on the supply of leading-edge and (to a lesser degree) legacy logic chips manufactured in China and Taiwan threatens U.S. economic and national security.

- U.S. consumption of logic is worth tens of billions of dollars per year, and an important minority (25 percent) of U.S. logic consumption goes toward more sensitive applications including artificial intelligence, data centers, and the military, as well as automotive applications (including military vehicles).
- Roughly 85 percent of global leading-edge 5 nanometers (nm) logic manufacturing capacity is located in Taiwan, and roughly 65 percent of global legacy (>16 nm) logic capacity is located in China and Taiwan. In the event of a conflict with China over Taiwan, the United States would likely lose access to all of this capacity. ○ The United States has zero onshore leading-edge (5 nm) logic capacity, and 8 percent of global legacy logic capacity above the 16 nm node.

Overdependence on the supply of dynamic random access memory (DRAM) chips manufactured in South Korea also poses risks.

- DRAM chips are also economically vital to the United States, but the country has minimal onshore DRAM manufacturing capacity and none at the leading edge.
- Half of global DRAM capacity is in South Korea, and most of the remainder (43 percent) is in Taiwan and China. South Korea faces moderate risks of disruptions in manufacturing due to its proximity to North Korea.

While the United States continues to lead in semiconductor design, the country has seen a consistent decline in semiconductor Assembly, Test, and Packaging (ATP) capacity. Though

there are several dozen U.S.-headquartered packaging vendors capable of providing boutique low-volume services, North America's share of global packaging capacity is only 3%. In general, U.S. firms (with the exception of Intel) lack high volume packaging capacity and the associated ecosystem (substrates, wafer bumping, equipment) is also lacking. Addressing this deficit should be prioritized. The costs of re-shoring advanced packaging necessitate a well-defined strategy. This strategy should make efficient use of funds to target specific technologies in the advanced packaging ecosystem, while accepting that the economics of re-shoring the broader ATP ecosystem prevent a return of meaningful capacity to the United States. This strategy should consist of three pillars:

- Increase advanced packaging facility capacity in the United States
- Increase supply of advanced packaging equipment and supplies in the United States
- Target research and development that supports innovation in advanced packaging

5. Subject to the criteria and eligibility requirements outlined in Section 9902 of the NDAA, what other factors should the Secretary consider as important when reviewing applications for Federal financial assistance?

In addition to the criteria and eligibility requirements outlined in Section 9902 of the 2021 NDAA, several important questions need to be addressed with respect to how applications for CHIPS Act incentives are considered. We recommend that policymakers provide answers to this non-exhaustive list of questions when crafting CHIPS Act incentive designs. These answers will provide clarity to firms interested in applying for funds and can help the U.S. government direct CHIPS Act funds to the highest-priority projects:

Covered Entities:

Pre-Existing Projects: Will fab expansion projects that are already underway be eligible for these incentives (e.g., Micron in Manassas, VA, Texas Instruments in Richardson, TX)?

CSET recommends that pre-existing projects be eligible for CHIPS Act funds provided they are not more than 25% complete.

GoCo Facilities: Are Government-Owned/Contractor-Operated (GOCO) facilities like Sandia National Lab's GaN fab and Brookhaven National Lab's rad-hard test facility eligible for incentives? If so, under what circumstances? Should there be an explicit FFRDC exclusion?

CSET recommends that GOCO facilities not be eligible for CHIPS Act funds except via funds designated for use under Section 9903 of the 2021 NDAA.

Eligibility Criteria:

U.S. HQ Preference: Should the incentives be firm headquarters-agnostic? (e.g., applications from Intel and TSMC would be reviewed on their merits without preference for the U.S.-headquartered company?)

CSET recommends that incentives distributed under Section 9902 of the 2021 NDAA be firm headquarters-agnostic. Indeed, CSET recommends that funds be specifically directed to incentivize the Taiwanese chipmaker TSMC to construct at least two leading-edge logic fabs in the U.S. and for the South Korean chipmaker Samsung to construct at least one leading-edge logic fab in the United States.

Multiple Applications: Can a company participate in more than one consortium application?

CSET recommends that companies be allowed to participate in more than one consortium that applies for CHIPS Act Funds.

Site Pre-Approval: Should site pre-approval (or lack thereof) affect a firm's eligibility for funds? How would applicants that have not secured state-level and federal-level approvals (e.g., NEPA) be treated?

CSET recommends that funds distributed under Section 9902 be preferentially directed towards projects which have secured some, but not necessarily all, state and federal permitting approvals to begin greenfield construction. Projects that apply for funds that have not secured any state or federal approvals should not be considered.

Bidding Categories:

Greenfield vs. Expansions: If there is a preference for boutique suppliers who plan to expand existing facilities vs. incentives for leading-edge suppliers who plan to build entirely new facilities that too may dictate consortium formation.

CSET recommends that Section 9902 incentives be directed towards large high volume greenfield fab construction projects and Section 9903 incentives be directed towards boutique DOD suppliers interested in expanding existing capacity.

Preference for Consortia Proposals that Address Multiple Supply Chain Vulnerabilities: If public and private entities are encouraged to partner on projects that "trickle down" (push funds to support Assembly, Test, and Packaging, or ATP) or "trickle up" (push funds to materials suppliers keen to co-locate with new fabs), this would also affect firm decision making. A higher score could be given to consortia who propose to distribute incentive funds to their upstream or downstream suppliers.

CSET recommends that preference be given to proposals that include construction of a leading-edge foundry AND a co-located advanced packaging facility. For example, if TSMC

were to build a back end fab adjacent to its front end fab in Arizona, that project should be preferentially considered eligible for Section 9902 funds above others.

DRAM incentives:

Incentives focused on DRAM chipmaking capacity should go to whichever firm can demonstrate the clearest long-term commitment to building capacity in the United States. DRAM fabs exhibit great economies of scale, such that establishing a single standalone DRAM is not economical: thus, DRAM firms should be expected to build not one but 3-4 fabs in the United States.

6. Section 9902 defines a covered entity to include, among other things public-private consortia, which could include partnerships between semiconductor firms and customers, suppliers, investors, state and local governments, federally funded research and development centers (FFRDCs), and other entities. How can Section 9902 incentives be designed and deployed to encourage additional and new private capital investment in the semiconductor ecosystem? What can be learned from other technology infrastructure development programs that use such partnerships (e.g., data center facilities or communications infrastructure) that may be applicable to semiconductor facilities?

7. How can federal financial assistance, consortia, or public-private partnerships be structured to maximize the initial scale of projects and to ensure ongoing reinvestment in project expansions, tool upgrades, and productivity improvements for the projects to remain economically viable and competitive over time? What opportunities exist for manufacturers to partner with private capital providers or use project financing to maximize the impact of the Federal financial assistance awards to achieve these objectives?

The Potomac Institute for Policy Studies, in a 2017 study on the effectiveness of microelectronics consortia such as SEMATECH, had a series of recommendations and findings that are responsive to questions 6 and 7. Several of these findings and recommendations are shared below.

Findings:

- Finding 1: Operational budgets need to be large enough, and stable over time, to match the size and scope of that organization's goals.
- Finding 2: A major cause of failure or delay in technology transition is due to a lack of willingness to fund later TRL stage development of promising technologies for DOD applications.
- Finding 3: A desirable near-term research direction for industry that would directly benefit the DOD is the development of low-volume manufacturing models.

- Finding 4: Other Transaction Agreements (OTAs) are specifically designed to be funding mechanisms for USG R&D and prototype programs.

The Potomac Institute for Policy Studies also provided several recommendations based upon these findings:

- Recommendation 1: Ensure that the funding level of any major public-private R&D initiative is at a magnitude that mirrors previous successful initiatives: $200-$300 million per year, 10-year timeline, total budget of $2-$3 billion.
- Recommendation 2: Include costs for technology transition and insertion in all major public-private R&D program budgets.
- Recommendation 3: Have government R&D efforts focus on low volume, customizable manufacturing solutions to technical challenges.
- Recommendation 4: Use OTA acquisition mechanisms in all R&D programs.

9. How can the program ensure that semiconductor startups and small- and mid-sized companies have access to commercial fabrication, assembly, testing and packaging facilities and associated technical expertise, including intellectual property products such as "Process Design Kits"?

In-Q-Tel released a report in 2021 that is responsive to this question. While the report is worth reading in full, among other things, it recommended:

- A national facility to field innovative semiconductor tools and fabricate next-generation microelectronics products in areas critical to national security. Variations on this idea have been called a microelectronics commons, a national semiconductor center, a Lab-to-Fab facility, and a hardware "sandbox." Such a facility could provide researchers and firms hands-on access to production lines that mirror commercial lines and can be adapted to explore new tooling capabilities, materials, components, and processes. The facility could also allow innovators to test and develop security assurance technologies on various devices and process flows.
- A fabrication sandbox could provide startups access to commercial equipment and tools, early design validation, and valuable testing data to share with potential investors while the government gains early access to innovative technology that could be tested against government requirements and inform future mission planning and acquisition needs.
- A dedicated Advanced Packaging facility that could test how U.S. chip designs work with Advanced Packaging processes and accelerate the transfer of technology from the lab, helping propel U.S. companies toward leadership in this emerging field. Compared to a leading-edge CMOS foundry, an advanced packaging facility will greatly impact how microelectronics will be designed in the future while costing orders of magnitude less.

10. Under the law, the Secretary may consider whether a covered entity includes a small business concern as defined under Section 3 of the Small Business Act (15 U.S.C. 632). Would it be beneficial for the Department to encourage large entities to partner with medium and small business suppliers?

The semiconductor industry is extremely capital intensive, and the number of small and medium sized businesses engaged in this industry is relatively small as a result. Partnerships between large established semiconductor firms and small emerging companies generally result in acquisition of the latter by the former. In addition, small and medium sized businesses in this industry are generally extremely specialized (e.g., they own a particular type of IP designed for AI chip optimization that a large firm may seek to license OR they are developing a specialized photoresist chemical required for semiconductor lithography). As a result, there are sufficient market-based incentives for large firms to partner with small firms when it fits within their business strategy. Encouraging partnerships between large and small firms is already happening in this industry, and both large and small firms are properly incentivized to continue these partnerships.

12. Section 9902 requires a covered entity to have secured commitments from regional educational and training entities and institutions of higher learning to provide workforce training to be eligible for funding. Looking at the semiconductor sector broadly, what are the greatest workforce development needs, and how can Federal financial assistance meet those needs? What specific types of workforce training programs would be the most beneficial to companies in these sectors? What existing workforce training programs have proven effective and should be expanded, including international exchanges or best practices? How could a program best ensure that workforce training and development meet critical national needs?

There are no “one size fits all” workforce development programs. DARPA’s JUMP program is responsive, but certainly not sufficient, to address the needs of the entire semiconductor industry. Programs that encourage pathways to employment for graduates of community and junior colleges, as well as those for degree holders in STEM fields, are essential.

Semiconductor workforce needs are divided by skill level, by firm, and by industry segment. For example, the semiconductor workforce needs of an equipment manufacturer like Applied Materials will be substantially different from the needs of an FPGA design firm like Xilinx. To make this point more explicit: semiconductor equipment manufacturers like Applied Materials, Lam Research, and KLA are in the business of physical assembly just as much as they are in the business of materials research, chemistry, and manufacturing. As a result, their workforce needs include a full spectrum from associates degree holders all the way to PhD materials scientists and engineers. In contrast, a firm like Xilinx is engaged in the business of FPGA design primarily, and its workforce needs are substantially differentiated. Xilinx requires bachelors, masters, and

doctoral degree holders in electrical engineering, physics, materials science, and chemistry, among others.

2. ADVANCED PACKAGING MANUFACTURING PROGRAM

CSET responses in this section draw in large part on a forthcoming paper related to advanced packaging. For any specific questions about the origins of the information presented in this section please contact the CSET POC listed in this RFI.

1. Please describe the application areas that are essential to long-term national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs.

Innovation in advanced packaging — including materials, equipment, and services — is essential to future U.S. semiconductor leadership. Innovations that increase semiconductor performance while reducing power consumption, cost, and form factor should be prioritized. In addition, innovations that are easily commercialized, flexible, and scalable, should be prioritized. Based on these factors, the United States should fund advanced packaging innovations related to chiplets and heterogeneous integration, equipment automation, and wafer-level packaging.

Chiplets and Heterogeneous Integration

As the costs of producing leading-edge chips has increased, the number of firms capable of producing such chips has decreased, and Moore's Law has slowed, chiplets have risen in popularity. According to one firm, the semiconductor industry is in the process of "adopting a chiplet based approach to reduce the overall cost, improve the individual yields and deliver required performance." Industry analysts expect that chiplets will be a key enabler of advances in semiconductors "for the next 10-20 years."

A chiplet "is an integrated circuit block that has been specifically designed to communicate with other chiplets, to form larger more complex ICs. Thus, in large and complex chip designs the design is subdivided into functional circuit blocks, often reusable IP blocks, called 'chiplets,' that are manufactured and recombined on high density interconnect."[3] In essence, chiplets are a way to make an electronic system behave like it is one integrated circuit when in fact it is composed of several different smaller integrated circuits. This is accomplished via heterogeneous integration, "the integration of separately manufactured components into a higher-level assembly (System in Package – SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics."[4]

Chiplets offer three main advantages: (1) Chiplets are small, allowing for greater operable dies per wafer, increasing the number of operable chips per wafer ("yield") and thus economies of

[3] https://eps.ieee.org/technology/definitions.html
[4] https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html

scale; (2) chiplets allow for heterogeneous integration of advanced and mature-node chips on the same system, collectively increasing system performance; and (3) customers can mix and match or customize various chiplets to optimize system performance for their specific applications.

Advanced packaging systems, materials, and equipment are all essential for enabling the die-to-die interconnects on which chiplets rely. While chiplets are not a package type, chiplets make use of advanced packaging to integrate different types of chips to form larger and more complex chips which have increased performance and functionality. Increasing adoption and consumption of chiplets will be contingent on advanced packaging innovations. AMD reports that its chiplet-based prototypes are 15% faster than its conventionally-packaged equivalent offerings.

Fan-Out Wafer-Level Packaging

Fan-out wafer-level packaging (FOWLP) refers to the process of packaging a finished semiconductor die while still in wafer form, either singly or combined with additional dies or other components such as discrete passive devices, or functional components like microelectromechanical systems (MEMS) or radio-frequency (RF) filters. This allows the production of wafer- and panel-level packaging using heterogeneous integration. The main advantages of FOWLP are the "substrate-less package, lower thermal resistance, higher performance due to shorter interconnects together with direct IC connection by thin film metallization instead of wire bonds or flip chip bumps and lower parasitic effects."

Interestingly, unlike other parts of the semiconductor supply chain, the supply chain for FOWLP is expanding. Analysts assess that there were ~5 firms engaged in FOWLP and this number has now grown to 11 in 2021. This technology is being adopted and popularized by TSMC in particular and is seeing increased adoption among its clients' systems as a result. As of 2020, TSMC maintained 66.9% market share for fan out advanced packaging and incentives should be directed to encourage TSMC to co-locate an advanced packaging facility with its Arizona fab to increase U.S. domestic capacity of wafer-level packaging capacity.

One example of FOWLP's benefits which is particularly relevant to AI comes from the U.S. chip startup, Cerebras. Cerebras designs so-called Wafer Scale Engines (WSEs), an application specific integrated circuit that encompasses an entire wafer and is optimized for machine learning tasks. However, even the fastest chips are constrained by the input/output capacity of their packaging. As a result, reports indicate that Cerebras is partnering with TSMC (its fabrication partner) to develop a wafer-scale package using TSMC's Fan Out process to preserve the size advantage/compute advantage that wafer-level processing creates and increase compute-related advances in artificial intelligence research and development. One U.S. Department of Energy laboratory reports that Cerebras' technology is providing modeling results

300x faster than its previous system. Further advances in how these WSEs are packaged would increase speeds and doing so in the U.S. would benefit innovative U.S. firms and U.S. government customers.

Advanced Packaging Equipment Innovation

As packaging techniques like FOWLP increase in popularity, the equipment and tools that support these packaging techniques must necessarily innovate to meet this demand. Importantly, these innovations in equipment also mean that packaging will become increasingly automated, which potentially changes the importance labor rates play in modeling future advanced packaging facility costs. In particular, wafer-level packaging places unique demands on equipment because it necessitates verification that the fabricated wafer contains the maximum number of operable chips. This quality control step was traditionally considered a “front end” semiconductor fabrication activity, but it is increasingly performed in support of “back end” advanced packaging requirements. These requirements have opened new business lines for large (primarily U.S.-based) suppliers of semiconductor manufacturing equipment who are now increasingly offering products to serve the advanced packaging market. One example of this is California-based KLA, a supplier of quality and process control equipment that leads the worldwide market for front-end metrology equipment used in semiconductor fabrication. KLA has recently started providing high-sensitivity defect detection tools for advanced wafer-level packaging.

Back-end advanced packaging increasingly resembles front-end semiconductor fabrication in terms of its need for automation. The more advanced packaging can be automated, the more U.S. equipment firms will benefit and labor rates will decrease as a deciding factor when firms choose where to locate Assembly, Test, and Packaging (ATP) facilities. The United States is poised to benefit from these trends and should make investments in support of it.

2. Please describe the R&D core-competencies that are essential to national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs.

Semiconductor packaging and semiconductor assembly are increasingly indistinguishable. As a result, success in semiconductor packaging requires close coordination between raw materials suppliers, component suppliers, and equipment suppliers, all of whom provide intermediate inputs that are used by firms (OSATs, IDMs, or foundries) that operate large, sterile, and increasingly-automated factories to process finished chips in preparation for their incorporation in to finished electronic products.

All of these suppliers represent core competencies essential to packaging leadership: materials, equipment, and packaging services. Assembly and packaging materials primarily consist of

substrates, ceramic packages, lead frames, and bonding wire. These materials are used to connect a fabricated chip to an encasing package, though the process and materials depend on the intended end use. Assembly and packaging equipment and tools are used to take completed wafers and transform them into packaged individual chips. Traditionally, this process is accomplished using equipment that inspects finished wafers, "dices" them into individual integrated circuits, bonds those individual integrated circuits to substrates, and packages those bonded ICs. Some advanced packaging techniques skip the process of dicing wafers and instead inspect them and bond them to a substrate before dicing in a process known as wafer-level packaging. Tools used in this process include assembly inspection tools, dicing tools, bonding tools, and integrated assembly tools. Packaging tools, a subset of assembly tools, consist of equipment used to encase and label dies in their protective cases; protect the dies from the environment; and handle the final packaging of assembled dies. Finally, OSATs, IDMs and foundries use the aforementioned materials and equipment to assemble and package finished wafers.

3. A proposed National Advanced Packaging Manufacturing Program could be oriented to address multiple needs, including but not limited to prototyping, the provision of pilot lines, workforce development, and supply chain development. Please describe the most critical needs on which the program should focus.

IC substrates are of particular importance to advanced packaging and U.S. firm presence and U.S. production in this market is extremely limited. IC substrates are used in a wide variety of electronics destined for aerospace and military applications in particular. The sole U.S.-based supplier of IC substrates suitable for advanced packaging reports that 36% of its total net sales (which also included IC substrates and printed circuit boards, among other electronic components) comes from the aerospace and defense market.

Within the supply chain for advanced packaging, there is a particularly acute shortage of the IC substrate material and certain types of equipment. Of particular concern are Ajinomoto Build Up film substrates. These substrates are used in packaging processes for high end CPU, GPU and 5G networking chips by major chipmakers, including Intel, AMD, and Nvidia. Fires in October 2020 at February 2021 Taiwanese producers of substrates exacerbated this supply crunch, leading to waits of up to 40 weeks for certain substrates.

Substrate suppliers are investing up to $5 billion in capacity expansion targeting FC-BGA substrate capacity, however new additional capacity will be available at the end 2022 at the earliest and it is all located outside the United States. An advanced substrate processing facility costs $300 million (Intel has estimated the cost to be $1 billion) and the equipment to operate such a facility currently has a two year lead time. In spite of the anticipated capacity expansions described in the above sections, one industry association estimates that this increased capacity will only be able to meet 78% of demand for these substrates in 2025.

One industry association found that the barriers to entry for the FC-BGA substrate market include a $1B+ investment needed, market leaders having a 20-year head start, and the need for a 1,000 person workforce per facility. Conversely, a South Korean PCB manufacturer recently opened a new facility in Malaysia at a cost of $121 million and reported that it will produce both PCBs and substrates. Given the increasing importance of substrates, some funds could be directed to encourage formation of one or more joint ventures (either between an OSAT and a substrate supplier, a foundry/IDM and substrate supplier, or a substrate and PCB supplier) to increase domestic production of IC substrates.

4. What attributes are the most important for a National Advanced Packaging Manufacturing Program to deliver?

The general observations highlighted by the Potomac Institute report highlighted earlier in CSET's response are relevant to advanced packaging well: the National Advanced Packaging Manufacturing Program should focus on placing bets on select technologies and consistently funding those priorities over a sustained period of time. The Potomac Institute report suggested $200-300M/year at a total budget of $2-3B on a 10-year timeline.

7. How closely aligned should the capabilities enabled by a National Advanced Packaging Manufacturing Program be with those provided by the NSTC?

These programs should be highly coordinated, as advanced packaging is an increasingly important driver of innovations in chip manufacturing more broadly.

8. How should the National Advanced Packaging Manufacturing Program connect to the National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA? What considerations should be given to ensure strong integration between the two efforts? Should there be overlap in the technology readiness levels served by each program?

The Department of Defense buys a wide variety of semiconductor devices, including both legacy and advanced chips. All chips require access to high-quality packaging to support DOD systems. As a particular packaging technology ascends Technology Readiness Levels, there should be increasing coordination between the programs.

3. SEMICONDUCTOR WORKFORCE

1. What are the greatest occupational or skills shortages facing employers in the semiconductor sector? What are the consequences of those shortages with respect to the domestic operation of employers in the sector? Considering all aspects of building, equipping, and running semiconductor manufacturing and R&D facilities, what actions have been taken to address these shortages, how effective have they been, and what gaps remain?

CHIPS Act manufacturing incentives will likely generate tens of thousands of new jobs, thousands of which will likely need to be filled by immigrants. Experienced, high-skilled foreign talent will be especially needed for engineering roles, where we have estimated that employment could grow by 19 percent over the next decade. Lower-skilled roles will see roughly 11 percent employment growth over the same period.

Estimated job growth generated by eight new fabs

Occupation	Estimated employment in semiconductor manufacturing industry	Estimated total growth (BLS projections + 27,000 jobs at eight new fabs)	Estimated growth as a percentage of current employment
Engineers and software developers	67,355	12,797	19%
Low-skilled technical workers	41,289	4,428	11%
Managers	6,622	524	8%
Other	69,734	6,607	9%
Total	185,000	24,356	13%

Source: CSET analysis of American Community Survey (ACS) Public Use Microdata Sample (PUMS), 2015-2019, and BLS data, 2019. Recreated from https://cset.georgetown.edu/publication/reshoring-chipmaking-capacity-requires-high-skilled-foreign-talent/, p.4

Fortunately, chipmakers are making long-term investments in workforce development in the regions where they are building new fabs. For example, to support the development of the new site, Intel has pledged $100 million toward partnerships with educational institutions to build a pipeline of talent and bolster research programs in the region. The United States could complement these efforts with investments in K-12 STEM education, funded 4+1 (undergrad + master's) programs in semiconductor-related fields, and on-the-job training programs to help

graduates acquire the tacit engineering know-how required for many semiconductor manufacturing-related careers.

However, these longer-term investments may not be sufficient to meet short-term talent needs. Semiconductor manufacturing firms have extensive and carefully-guarded engineering know-how required for making chips, particularly chips at the leading edge. This know-how can be transmitted to others, but it requires extensive and costly direct instruction: foreign firms like TSMC are currently transporting American workers to Taiwan in order to train them in TSMC's manufacturing processes. We estimate that a significant number of experienced foreign-born workers, particularly with software development and engineering backgrounds, will need to immigrate to the United States to support the establishment of new fabs.

Estimated foreign workers required to staff eight new fabs

Broad occupation	Percentage of non-U.S. citizens in semiconductor industry	Estimated foreign workers needed to staff eight fabs
Engineers and software developers	22%	2,356
Low-skilled technical workers	11%	384
Managers	9%	67
Other	11%	745
Total	14%	3,552

Source: CSET analysis based on ACS PUMS data and BLS data. Recreated from https://cset.georgetown.edu/publication/reshoring-chipmaking-capacity-requires-high-skilled-foreign-talent/, p.11

Policymakers should therefore consider establishing an accelerated immigration pathway for experienced fab workers—perhaps specifically for Taiwanese or South Korean workers seeking to work in newly constructed fabs in the United States. Caps on employment-based green cards should also be lifted for workers in the semiconductor industry, or perhaps for workers in national-security-relevant industries more broadly, if those workers have relevant master's or doctoral degrees. This will be particularly helpful for U.S. firms like Intel which currently employ many workers using employment-based green cards.